USC Viterbi School of Engineering

EE 457 Computer Systems Organization

Units: 4

Spring 2025 - Mon. Wed. 2:00-3:50 PM in OHE230
and Tues. Thurs. 4:00-5:50PM in OHE100D

Instructor: Gandhi Puvvada
Office: EEB 238;
Gandhi's office hours: Gandhi_Office_Hours_Sp2025.pdf
55 min on **Mondays evening 4:05-5:00 PM in OHE336**. In person + Zoom 684 224 6098
45 min on **Tuesdays morning 9-9:45 AM**. On Zoom only 684 224 6098
35 min on **Tuesdays and Thursdays 5:55-6:30 PM in OHE100D**. In person + Zoom 684 224 6098
65 min on **Wednesdays 3:55 to 5:00 PM in OHE230**. In person + Zoom 684 224 6098
35 min on **Thursdays 5:55-6:30 PM in OHE100D**. In person + Zoom 684 224 6098

Contact Info: gandhi@usc.edu, (preferred)
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(for occasional urgent needs)

Teaching Assistant:
EE457 TA -- Dongyang Wu <wudongya@usc.edu>

Course CPs: TBA

TA/CP's Office: Zoom/PHE330
Office Hours of TAs and CPs TBA

1. Course Description

This course covers computer organization and design. It provides CS/CE/EE students with a substantial understanding of a CPU at its logic design level. Design of the control unit and the data path unit of a simple multi-clock-cycle CPU and a pipelined CPU is covered in detail. Computer arithmetic and memory hierarchies (cache, main memory, virtual memory) are also covered. Hardware support for exceptions, dynamic scheduling of instructions (Tomasulo algorithm to execute instructions in an out-of-order fashion), branch prediction, multi-threaded cores, multi-core processors with cache coherency, locks and mutual exclusion among threads via special atomic instructions are also discussed in detail. Students design in Verilog and use ModelSim simulator to verify their RTL design/simulation exercises.

2. Learning Objectives

At the end of the course, students are expected to feel confident to perform logic design of a CPU or any hardware system utilizing pipelining and other RTL design techniques and proceed to graduate courses in computer architecture or general hardware design. This course is also expected to improve students' design and analytical skills.

3. Course administration

a) Course prerequisites: EE354L (previously EE254L or EE201L) Introduction to Digital Circuits is a *necessary* prerequisite. Undergraduate students without this prerequisite will not be able to do this course. Graduate students are expected to have taken a logic design course and a course covering some assembly language in their undergraduate course work before taking this course.

Recommended Preparation: Familiarity with the following items at an introductory level is expected.

1. Programming in an assembly language of any processor (CISC or RISC)
   General Purpose Registers, Program Counter, Conditional branches, Call and Return instructions involving stack operations, exceptions and interrupts
2. Digital Logic design at RTL level (Register Transfer Language Level)
   Small System Design involving a Datapath unit and a Control Unit, ALU design, Timing Design, Waveform drawing and interpretation
3. Design entry using Verilog HDL (Hardware Description Language) and simulation
   Event-driven simulation and the delta-T concept, representation of concurrency using instantiations, concurrent *assign* statement, *always* procedural blocks, use of blocking and non-blocking assignments in procedural blocks (blocks with a *begin* and an *end* where sequential statements are used), Testbenches

b) Classes: https://classes.usc.edu/term-20251/course/ee-457/

Discussion class is *not optional*. Homework and lab assignments are primarily discussed during the discussion class. Important additional material may be covered in the discussion class.

c) Examinations: No makeup exams.

Please note that EE457 exams are long (3 Hours) as they are design exams.

One quiz (~11%), one midterm (~25%), and one final exam (~34%)
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Quiz (~11%): Friday, Feb. 14, 2025, 05:00 PM - 08:00 PM PST
Midterm (~25%): Friday, Mar. 28, 2025, 05:00 PM - 08:00 PM PST
Final Exam (~34%): Wednesday, May 14, 2025, 03:30 PM - 06:30 PM PST **Please check**
Official slot of 4:30-6:30PM extended by an hour

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The "Quiz" slot (Qz 5:00-7:50PM Friday)
We will utilize this slot only twice in the whole semester to conduct a quiz and a midterm exam.
So, it is OK to have a schedule conflict with the quiz slot provided you agree to make yourself available for these two occasions.

Quiz (~11%): Friday Feb. 14, 2025, 05:00 PM - 08:00 PM PST
Midterm (~25%): Friday Mar. 28, 2025, 05:00 PM - 08:00 PM PST

Feb. 28 (Friday)? Please verify	Last day to drop a class without a mark of "W"
April 11 (Friday) ? Please verify	Last day to drop a class with a mark of "W"

https://classes.usc.edu/term-20251/registration-calendar/

Note: EE457 Final Exam is listed under the Exceptions Schedule posted at the bottom of:
https://classes.usc.edu/term-20251/final-examinations-schedule/

Electrical Engineering 457	Wednesday, May 14	4:30-6:30 p.m.

I propose that the time is extended by 1 hour by starting the exam 1 hour early (i.e., 3:30 PM instead of 4:30 PM)] as shown below to allow a 3-hour exam.
Final Exam (about 34%): Wednesday, May 14, 2024, 3:30 PM - 6:30 PM PST
Official slot is 4:30 PM to 6:30 PM. With your cooperation, I want to start the exam early by 1 hour at 3:30 PM.
I have checked the final exam schedule and reproduced below the adjacent exams' schedule with potential conflict.

12 or 12:30 or 1 TTh	Wednesday, May 14	2-4 p.m.

I hope that none of our EE457 students are taking a course starting at 12 noon or 12:30 PM or 1 PM TTh. We will reconfirm with all our students to make sure that this works for everyone. Please let me know if you have any time conflict because of this time extension (**early start of the final exam at 3:30 PM on Wed. May 14th**).

d) Grading Policy:

Course weights			
Assignments	**percentage**		Late submission penalty for assignments
Homeworks (short and long) (Individual work)	about 6%		5% penalty per day for long homeworks up to 3 days if solution is not given out. For short homeworks, solution is given away at the time of the assignment. 5% penalty per day up to 3 days for short homeworks also.
Labs (some Individual and some Teamwork)	about 23% to 25%		3% flat penalty up to 3 days for online code submissions. 5% penalty per day up to 1 day for Lab paper submission
Exams	Scale1	Scale2	
Quiz	10%	12%	**no make-up exam**
Midterm	23%	27%	**no make-up exam**
Final	37%	31%	**no make-up exam**
Attendance is noted based on in-person attendance. DEN Remote students are allowed to watch the lectures synchronously or asynchronously on Zoom.			
Penalty for lecture absence: 0.5% of the course for the 5th and the 6th; 1% for the 7th and thereafter			
Penalty for discussion absence: 0.5% for the 5th and the 6th; 1% for the 7th and thereafter			

e) Academic Accommodations:

Any student, requiring academic accommodations based on a disability, is required to register with the **Office of Student Accessibility Services (OSAS)** each semester.
An online profile can be created on **MyOSAS** .
A letter of verification for approved accommodations can be obtained from OSAS.
Please make sure that the letter is delivered to me as early in the semester as possible
(no less than **2 weeks** before an exam).
The OSAS office is located in GFS 120.
Their phone number is (213) 740-0776. Email: **osasfrontdesk@usc.edu**
https://osas.usc.edu/new-students/main-facilities/

f) Miscellaneous administrative matters:

Lecture class attendance, penalty for absence, and minimum required performance:

If you miss more than 2 lecture meetings, you will start noticing that you are falling behind.
If you miss more than 5 lecture meetings, you may as well drop the course.
It is a design course requiring continuity in your learning process. So, please attend every lecture/discussion meeting.
Attendance is noted based on physical attendance for sections 30478D and 30591D for lecture and 30593R for discussion.
Penalty for lecture absence: 0.5% for 5th, 6th; 1% for 7th and after.
Penalty for discussion absence: 0.5% for 5th, 6th; 1% for 7th and after.
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/EE457_attendance_policy.html
The DEN remote students (registered in sections 30595D and 30594D) are allowed to watch the lecture and discussion synchronously or asynchronously in the evening/late night. But they should finish watching lectures/discussion of a week within that week and send an email to the TA and me stating that they watched the week's lectures and discussion before the end of the next Monday.
Homeworks and *short homeworks, posted on Brightspace/Gradescope,* shall be done individually. Design and simulation labs: Some of these are individual assignments and some are team assignments. See the

EE457_due_dates_Calendar_Sp2025.pdf to find which lab assignment is an individual assignment and which is a team-effort assignment. Team assignments can be performed either individually or in teams of two students (2 per team).
Teams shall submit only one set of Verilog code and results online from one student's Unix account. The two students in a lab team shall not submit separately as such duplicate submission is similar to to submitting two answers for one question in an exam and asking the instructor to choose the right answer to grade!
However, justifications/explanations, state diagrams, and answers to questions at the end of the lab assignment (called **paper submissions), shall be prepared individually (and not as a team).**
Copying is different from discussing ideas with other students.
You are encouraged to share your thoughts on all items of the course (homeworks, short homeworks, design labs, and design lab reports) with other students as long as one of you act as a *Teaching Assistant* who tries to help without giving away the solution. Of course, exams are completely individual (I do not need to say this!).

Absolutely no copying. Do NOT try to copy any assignment. We have ways to find if a design/simulation lab or some homework has been copied.
Try not submitting a non-working lab as we give very little credit for a non-working lab.
We are here to help you and guide you in how to approach a lab (and sometimes help you in your debugging also).
If you submit a **non-working design/lab** and if you do not write on the top of it in **BIG** letters that it is NOT WORKING (and further do not inform the TA and/or the graders through an email before submission), we will treat it as an attempt to cheat. This is very important.

Academic dishonesty cases will be dealt with severely.

We will try to make the assignments due on times far from the class time (usually 11:59 PM PST).
This is to make sure that students do not miss classes to complete their assignments.

Please check your email regularly. Please check if the emails sent by me (either directly or via Brightspace) go to your SPAM email folder. Also visit the Brightspace regularly at https://brightspace.usc.edu/d2l/home .
Exam related information, office hours, and due dates for assignments are all posted on Brightspace => Contents => Announcements and also in the directory:
https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/ee457_Sp2025_exams/

Academic dishonesty cases will be dealt with severely. Please go through the short tutorial on Academic Integrity at USC posted at
https://libraries.usc.edu/research/reference-tutorials
https://libraries.usc.edu/tutorial/academic-dishonesty

Please refer to pages 11-13 of The USC Student Handbook covering academic integrity.
https://policy.usc.edu/wp-content/uploads/2023/09/USC_StudentCode_September2023-1.pdf

University policy requires that all academic integrity violations are reported to Student Judicial Affairs and Community Standards (SJACS) if the student is an undergraduate and to the VSoE if the student is a graduate student.

We will try to make the assignments due on times far from the class time (usually 11:59 PM PST).
This is to make sure that students do not miss classes to complete their assignments.

4. Design/simulation labs sequence:

Approximately one lab (or one part of one lab) will be assigned every week starting from the second week.
The labs make up about **24%** of your course credit.

0) Introduction to Verilog HDL entry and simulation in Modelsim

1) Max. Min. finder State Machine Design Lab #1 Part #1, Part #2, Part #3 (M1, M2, ~~M3, M4~~)

2) Design of a 32-bit ALU Lab #3

3) FIFO ~~and its application~~

4) Pipeline labs
Design of a 3-element adder Lab #7 Part #1, #2,
Design of a simple pipeline Lab 7 Part #3 (Sub parts SP1, SP2)
RTL Coding of a simple pipeline Lab 7 Part #3 (Sub parts SP3, ~~SP4~~)

5) Design of a Pipelined CPU Lab #6 Part #4 and Part #5 (only paper submissions)

5. Readings:

The required readings are class notes and sections of the textbook. Please make it a practice to read regularly. It is important to clarify any items that are not clear in that week itself. Students, who postpone reading, gradually drift away from the rest of the class, and eventually perform very poorly on the exams and design/simulation labs.

Primary References:

Class Notes (required): ~~Please buy from the university (USC) bookstore~~. Please access it online.

Lab Manual: Individual labs are posted on the ee457 Brightspace page.

Textbook/Verilog Guide:
1. Computer Organization & Design - MIPS Edition - The Hardware and Software Interface 5th edition
By D. A. Patterson (Berkeley) and J. L. Hennessey (Stanford)
We do not use the textbook that much. Some students manage without the textbook. But this is a very good book to buy and keep.
You can buy it from the university (USC) bookstore or any place (such as online bookstores).
http://store.elsevier.com/Computer-Organization-and-Design/David-Patterson/isbn-9780124077263/
If you have the 4th edition, that is fine too.

2. The Verilog 2001 Reference Guide by Esperan (Cadence)
You need this for your Verilog-based design/simulation labs. **However you cannot use it in the EE457 exams**. Esperan (Cadence) does not sell it to individuals. They provided the pdf file to us free. It is posted on the Brightspace. Please do not redistribute or repost it anywhere.

Secondary References (Do not buy these):

1. EE354L (previously called EE254L/EE201L) Textbook: Digital Design Principles and Practices by John F. Wakerly
2. EE557 Textbook: Parallel Computer Organization and Design by Dubois, Annavaram, and Stenstrom
3. Computer Architecture - A Quantitative Approach by D. A. Patterson and J. L. Hennessy

6. An approximate Course Schedule by week for Spring 2023:
Chapter numbers point to chapters in my class notes (https://viterbi-web.usc.edu/www-classes/engr/ee-s/457/EE457_Classnotes/).
Homeworks and labs are due generally 1 week after they are assigned.
Due dates calendar has been posted.

# of lectures	Lecture #	Item	Homework /Lab
2	1, 2 Week #1 1/13-1/17	**Ch#1** Intro to course, review of prerequisite material, Review data path and control unit design, Moore and Mealy, Glitches in control signals, Data registers with Data enable, State diagram design, All Inclusive and Mutually Exclusive rules, Concurrent RTL operations in RTL design. welcome.pdf, 1_microarchitecture.pdf, DPU_CU.pdf, 3_Moore_Mealy_Divider.pdf, 4_Data_Registers.pdf, 5_P1_loop_counter.pdf, 5_P2_loop_counter.pdf, 5_P3_loop_counter.pdf, 6_P1_mutually_exclusive.pdf, 6_P2_ME_AI_tables.pdf, 7_State_Diagram_Design_examples.pdf	HW#1 H1.pdf RL.pdf HW#1A for practice H1A.pdf HW1A_sol.pdf HW#1B HW1B.pdf HW1C_prelude.pdf HW1C_assign.pdf
0		Verilog coding: Watch the 6-part EE354L lectures at home and learn by yourselves. Install Modelsim/Questasim and learn to use the tool by yourself	Tools installation and/or VDI
1	3 Week #2 1/20-1/24	Compare and contrast: state diagram vs. flow-chart, Min-Max (a 4-part lab: P1, P2, P3-Method1, P3-Method-3)	Lab #1
1	4 Week #2 1/20-1/24	**Ch#2** Performance, MIPs, MFLOPs ch2.pdf Amdahl_Law.PDF pdf	HW #2 HW2.pdf
2.5	5, 6, Week #3 1/27-1/31	**Ch#3** MIPs ISA, SLT, SLTU lw, sw, Byte addressable processors, memory addresses. also cover word addresses in a byte addressable processor P1.pdf, P2.pdf, addr_space_exer.pdf, addr_space_sol.pdf, Quiz_Sp2019_sol_Q4 (.pdf, .mp4) HW#3 (exer.pdf, sol.pdf, disc.pdf, disc.avi) HW4page2.pdf	
1.5	7, 8 Week #4 2/3 – 2/7	**Ch#4 P1** Review overflow detection in unsigned and signed arithmetic and ALU design P1.pdf, ~~p1.pdf~~, ee560_HW0_ques_adder.pdf	ALU lab Lab #3
1	9 Week #5 2/10-2/14	**Ch#5 P1** Single Cycle CPU,	HW #5A (Single-cycle CPU)
1	10 (no lecture) Week #5 2/14	**Quiz exam** **on Friday Feb. 14, 2025, 5:00 PM-8:00 PM in Room: _____**	Quiz Room: TBA
~~0~~	~~11, 12~~ ~~Week #6~~ ~~2/12-2/16~~	~~Ch#5 P2 multi-cycle CPU Datapath and control design~~ ~~Ch#5 P2 Multi-cycle CPU 2nd edition design~~ During recent semesters, we were skipping this topic.	~~Lab 4 Part #4 (Multi-cycle CPU)~~ ~~(paper submission)~~ ~~HW #5B~~ ~~(Multi-cycle CPU)~~
5	11,12, 13, 14, 15 Week #6,#7,#8 2/17-3/4	Ch#6 5-stage pipeline: data dependency solutions (Compiler solution, HDU & FU), and branch implementations (late branch vs. early branch), branch delay slots. Also cover exceptions. Links to pipeline topics (very important)	Pipelining Lab 6 – Part 4 (paper submission)
		LAB 7 Parts 1&2 (PIPELINED 3-ELEMENT ADDER) https://ece-classes.usc.edu/ee457/ee457_lab_manual_Fl2010/ee457_lab7_P1/	FIFO lab
2	16, 17,18 Week #8,#9 3/5-3/11	Ch#7 P1 Cache: Mapping techniques, CPU address division into fields and connect address to Cache Data RAMs, Cache Tag RAMs.	Cache HW #6 Pipeline lab #7 P1 and P2 paper

1	3/12-3/13	Ch#7 P2 Virtual memory: multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory	
	Week #10 3/16-3/22	Spring Recess March 16-23	
1	19 Week #11 3/24-3/25	Ch#7 P2 Virtual memory (continuation): multi-level page table, PTBR, principle of inclusion. TLBs, and interleaved main memory	
1	20 (no lecture) Week #11 3/26-3/27	**Midterm exam on Friday March 28, 2025, 5:00 PM-8:00 PM in Room: _____**	MT room: TBA
2	21, 22 Week #12 3/31-4/4	Discussion covers Exceptions, Brach Prediction, 1-bit and 2-bit predictors, BPB, BTB, OoO Intro.	Virtual Memory HW #7
2	23, 24 Week #13 4/7-4/11	Out of order execution and Tomasulo Part 1 (IoI_OoE_OoC), WAR and WAW hazards in OoO execution, IFQ (Instruction prefetch queue), dispatch unit, issue queues, issue unit, CDB, ROB	Lab #7 P3 Sub Parts 1, 2 (paper submission)
2	25,26 Week #14 4/14-4/18	Tomasulo Part 2 (IoI_OoE_IoC), ROB, ROB search, Speculative execution and selective flushing if branch was mispredicted, exception handling, Intro to the remaining topics	~~ROB lab~~
2	27, 28 Week #15 4/21-4/25	Ch#9 Parallel processing, semaphores, Read-Modify-Write (RMW) race, atomic operations on shared variables, CMP, Snoopy Cache Coherency protocols, Write through vs. write-back, MSI, MOESI	Pipeline RTL coding lab Lab #7 P3 Sub Parts 3, 4
1	29 Week #16 4/28-4/29	CMT, Thread-level parallelism, non-blocking cache, MPI	
1	30 Week #16 4/30-5/1	Locks, Atomic operations, LL and SC instructions in MIPs	
		Classes end on May 2, 2025, Friday. Study Days May 3-6 USC Spring 2025 calendar	
		Final exam on Wednesday, May 14, 2025, 3:30 PM to 6:30 PST Official slot of 4:30-6:30 PM is extended by 1 Hr. Please see the exceptions list at the bottom of https://classes.usc.edu/term-20251/final-examinations-schedule/ Electrical Engineering 457 Wednesday, May 14 4:30-6:30	Final exam slot extended by one hour. **Starts at 3:30 PM**

Statement on Academic Conduct and Support Systems

Plagiarism – presenting someone else's ideas as your own, either verbatim or recast in your own words – is a serious academic offense with serious consequences. Please familiarize yourself with the discussion of academic integrity in "The USC Student Handbook" on pages 11 through 13. Other forms of academic dishonesty as described in the Student Handbook are equally unacceptable.

Counseling and Mental Health - (213) 740-9355 – 24/7 on call
https://studenthealth.usc.edu/counseling
Free and confidential mental health treatment for students, including short-term psychotherapy, group counseling, stress fitness workshops, and crisis intervention.

988 Suicide & Crisis Lifeline - 988 or 1 (800) 273-8255 – 24/7 on call
https://988lifeline.org
Free and confidential emotional support to people in suicidal crisis or emotional distress 24 hours a day, 7 days a week.

Relationship and Sexual Violence Prevention Services (RSVP) - (213) 740-9355(WELL), press "0" after hours – 24/7 on call
https://studenthealth.usc.edu/sexual-assault
Free and confidential therapy services, workshops, and training for situations related to gender-based harm.

Office of Equity and Diversity (OED) - (213) 740-5086 | **Title IX –** (213) 821-8298
https://equity.usc.edu, https://titleix.usc.edu
Information about how to get help or help someone affected by harassment or discrimination, rights of protected classes, reporting options, and additional resources for students, faculty, staff, visitors, and applicants.

Reporting Incidents of Bias or Harassment - (213) 740-5086 or (213) 821-8298
https://usc-advocate.symplicity.com/care_report
Avenue to report incidents of bias, hate crimes, and microaggressions to the Office of Equity and Diversity |Title IX for appropriate investigation, supportive measures, and response.

Office of Student Accessibility Services (OSAS) - (213) 740-0776 (previously called Disability Services and Programs (DSP)) https://osas.usc.edu
Support and accommodations for students with disabilities. Services include assistance in providing reader- s/notetakers/interpreters, special accommodations for test taking needs, assistance with architectural barriers, assistive technology, and support for individual needs.

USC Campus Support and Intervention - (213) 821-4710
https://campussupport.usc.edu
Assists students and families in resolving complex personal, financial, and academic issues adversely affecting their success as a student.

Diversity at USC - (213) 740-2101
https://diversity.usc.edu
Information on events, programs and training, the Provost's Diversity and Inclusion Council, Diversity Liaisons for each academic school, chronology, participation, and various resources for students.

USC Emergency - UPC: (213) 740-4321, HSC: (323) 442-1000 – 24/7 on call
https://dps.usc.edu, https://emergency.usc.edu
Emergency assistance and avenue to report a crime. Latest updates regarding safety, including ways in which instruction will be continued if an officially declared emergency makes travel to campus infeasible.

USC Department of Public Safety - UPC: (213) 740-6000, HSC: (323) 442-120 – 24/7 on call
https://dps.usc.edu
Non-emergency assistance or information.

Office of the Ombuds - (213) 821-9556 (UPC) / (323-442-0382 (HSC)
https://ombuds.usc.edu
A safe and confidential place to share your USC-related issues with a University Ombuds who will work with you to explore options or paths to manage your concern.